

## **REMARKS**

The present application is a Rule 1.53(b) Continuation Application of pending U.S. Application Serial Number 09/148,392, which was filed on September 4, 1998. Claims 1-27 are pending in the application. In the final Office Action mailed September 12, 2000, the Examiner objected to the abstract, objected to the drawings, provisionally rejected Claims 1-27 under 35 U.S.C. § 101 for double patenting, and rejected Claims 1-27 under 35 U.S.C. § 102. Applicant has canceled claim 21, and has amended Claims 1, 4, 10-12, 14, 17-20, 22-23, and 25. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

### **I. TITLE**

In the Office Action, the examiner objected to the amended title. In particular, the Examiner stated that the title of the invention is not descriptive. In response, Applicant has amended the title to change to SELECTING DESIGN POINTS FOR PARAMETER FUNCTIONS TO OPTIMIZE DESIGN PARAMETERS WITHIN DESIGN CONSTRAINTS.

Therefore, Applicant respectfully requests the objection to the title be withdrawn.

### **II. ABSTRACT**

In the Office Action, the Examiner objected to the Abstract. In response, Applicant has amended the Abstract to recite the novelty of the invention. Therefore, Applicant requests the objection to the Abstract be withdrawn.

### **III. REJECTIONS UNDER 35 U.S.C. § 102**

In the Office Action, the Examiner rejected Claims 1-27 under 1) 35 U.S.C. § 102(e) as clearly anticipated by U.S. Patent No. 5,838,947 issued to Sarin ("Sarin") or U.S.

Patent No. 5, 880,967 issued to Jyu et al. ("Jyu"), 2) under § 102(a) as being clearly anticipated by U.S. Patent No. 5,835,380 issued to Roething ("Roething") and 3) under § 102(b) as being clearly anticipated by U.S. Patent No. 5,619,420 issued to Breid ("Breid"). Applicant respectfully traverses the rejections for the following reasons.

Applicant reiterates the arguments against the rejections as set forth in the previous response. In particular, Applicant submits that Sarin, Jyu, Roething and Breid, taken alone or in any combination, do not disclose, suggest, or render obvious (1) creating parameter functions for a plurality of circuits in the subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits, (2) selecting initial design points for the parameter functions to satisfy the design constraints; and (3) selecting new design points for the parameter functions to optimize design parameters within the design constraints. These aspects of the invention are supported in the specification on page 18, lines 6-23, pages 19-20, and page 21 (lines 1-15), and are recited in the amended Claims 1, 11, and 22.

Applicant has also amended Claims 1, 4, 10-12, 14, 17-20, 22-23, and 25 to correct minor informalities not previously recognized and to clarify the claim language.

Therefore, Applicant believes that independent Claims 1, 11, and 22 and their respective dependent Claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. § 102(b) be withdrawn.

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE ABSTRACT**

Please delete the Abstract and insert the following in lieu thereof

--One embodiment of the present invention is a method and machine readable medium for determining optimal values of design parameters of a subsystem to meet design constraints. The subsystem includes a number of circuits. A parameter function is created for the corresponding circuits. The parameter function represents a relationship among the design parameters. Initial design points for the parameter functions are selected to satisfy the design constraints. New design points for the parameter functions are selected to optimize design parameters within the design constraints--.

**IN THE CLAIMS:**

- 1           1.       (TWICE AMENDED) A method comprising:
- 2                       (a) creating parameter functions for a plurality of circuits in a subsystem, the
- 3                       subsystem having design constraints, each one of the parameter functions
- 4                       corresponding to each one of the circuits, the parameter functions representing a
- 5                       relationship among the design parameters; [and]
- 6                       **(b) selecting initial design points for the parameter functions to satisfy the**
- 7                       **design constraints; and**

8                    [(b) optimizing design parameters based on the parameter functions to  
 9                    satisfy] (c) selecting new design points for the parameter functions to optimize  
 10                    design parameters within the design constraints.

1            2.        The method of claim 1 wherein the creating the parameter functions  
 2                    comprises:

3                    (a1)    configuring each circuit of the plurality of circuits; and

4                    (a2)    generating values of design parameters for each circuit according to  
 5                    the configured circuit, the values providing the parameter functions.

1            3.        The method of claim 2 wherein the design parameters include constraint and  
 2                    optimizing sets, the constraint set including constraint parameters having values selectable  
 3                    to meet the design constraints, the optimizing set including optimizing parameters having  
 4                    values to be optimized.

1            4.        (AMENDED) The method of claim 3 wherein [optimizing] selecting the  
 2                    new design points comprises:

3                    [(b1)] (c1)    selecting values of the constraint parameters to meet the  
 4                    design constraints;

5                    [(b2)] (c2)    determining values of the optimizing parameters  
 6                    corresponding to the selected values of the constraint parameters based on the  
 7                    parameter functions; and

8                    [(b3)] (c3)    iterating [(b1)] c(1) and [(b2)] (c2) until values of the  
9                    optimizing parameters are within a predetermined optimal range.

1                    5.        The method of claim 3 wherein the constraint parameters include a delay  
2                    parameter and the optimizing parameters include a power parameter.

1                    6.        The method of claim 5 wherein the design constraints include a delay  
2                    constraint.

1                    7.        The method of claim 6 wherein (a1) comprises:  
2                    sizing components in each circuit.

1                    8.        The method of claim 6 wherein (a1) comprises:  
2                    selecting a design technology for each circuit, the design technology being one of  
3                    static and dynamic technologies.

1                    9.        The method of claim 7 wherein (a2) comprises:  
2                    (a21)    generating a circuit netlist representing the configured circuit;  
3                    (a22)    generating a timing file based on the circuit netlist using a circuit  
4                    critical path;  
5                    (a23)    determining power of the configured circuit based on the circuit  
6                    netlist;

7 (a24) calculating timing values by using a timing simulator; and

8 (a25) calculating power values by using a power estimator.

1 10. The method of claim 9 wherein [optimizing] selecting the new design points  
2 comprises:

3 [(b1)] (c1) selecting values of the delay parameter within the delay  
4 constraint;

5 [(b2)] (c2) determining values of the power parameter corresponding to  
6 the selected values of the delay parameter based on the parameter function; and

7 [(b3)] (c3) iterating [(b1)] (c1) and [(b2)] (c2) until values of the power  
8 parameter are within a predetermined optimal range.

1 11. (TWICE AMENDED) A machine readable medium having embodied  
2 thereon a computer program for processing by a machine, the computer program  
3 comprising:

4 (a) a first code segment [for creating] to create parameter functions for a  
5 plurality of circuits in a subsystem, the subsystem having design constraints, each  
6 one of the parameter functions corresponding to each one of the circuits, the  
7 parameter functions representing a relationship among the design parameters; [and]

8 (b) a second code segment to select initial design points for the  
9 parameter functions to satisfy the design constraints; and

10                    [(b)] (c)            a [second] third code segment [for optimizing design  
 11 parameters based on the parameter functions to satisfy] to select new design points  
 12 for the parameter functions to optimize design parameters within the design  
 13 constraints.

1            12.        (AMENDED) The machine readable medium of claim 11 wherein the first  
 2 code segment comprises:

3                    (a1)    a code segment [for configuring] to configure each circuit of the  
 4 plurality of circuits; and

5                    (a2)    a code segment [for generating] to generate values of design  
 6 parameters for each circuit according to the configured circuit, the values providing  
 7 the parameter functions.

1            13.        The machine readable medium of claim 12 wherein the design parameters  
 2 include constraint and optimizing sets, the constraint set including constraint parameters  
 3 having values selectable to meet the design constraints, the optimizing set including  
 4 optimizing parameters having values to be optimized.

1            14.        (AMENDED) The machine readable medium of claim 13 wherein the  
 2 [second] third code segment comprises:

3                    [(b1)] (c1)            a code segment [for selecting] to select values of the  
 4 constraint parameters to meet the design constraints;

5            [(b2)] (c2)    a code segment [for determining] to determine values of the  
 6            optimizing parameters corresponding to the selected values of the constraint  
 7            parameters based on the parameter functions; and

8            [(b3)] (c3)    a code segment [for iterating (b1)] to iterate (c1) and [(b2)]  
 9            (c2) until values of the optimizing parameters are within a predetermined optimal  
 10           range.

1           15.    The machine readable medium of claim 13 wherein the constraint  
 2           parameters include a delay parameter and the optimizing parameters include a power  
 3           parameter.

1           16.    The machine readable medium of claim 15 wherein the design constraints  
 2           include a delay constraint.

1           17.    (AMENDED) The machine readable medium of claim 16 wherein (a1)  
 2           comprises:

3           a code segment [for sizing] to size components in each circuit.

1           18.    (AMENDED) The machine readable medium of claim 16 wherein (a1)  
 2           comprises:

3           a code segment [for selecting] to select a design technology for each circuit,  
 4           the design technology being one of static and dynamic technologies.



1 19. (AMENDED) The machine readable medium of claim 18 wherein (a2)  
2 comprises:

3 (a21) a code segment [for generating] to generate a circuit netlist  
4 representing the configured circuit;

5 (a22) a code segment [for generating] to generate a timing file based on  
6 the circuit netlist using a circuit critical path;

7 (a23) a code segment [for determining] to determine power vectors of the  
8 configured circuit based on the circuit netlist;

9 (a24) a code segment [for calculating] to calculate timing values; and

10 (a25) a code segment [for calculating] to calculate power values.

1 20. (AMENDED) The machine readable medium of claim 19 wherein the  
2 [second] third code segment comprises:

3 [(b1)] (c1) a code segment [for selecting] to select values of the delay  
4 parameter within the delay constraints;

5 [(b2)] (c2) a code segment [for determining] to determine values of the  
6 power parameter corresponding to the selected values of the delay parameter based  
7 on the parameter function; and

8 [(b3)] (c3) a code segment [for iterating (b1)] to iterate (c1) and [(b2)]  
9 (c2) until values of the power parameter are within a predetermined optimal range.

1           21.    (CANCELED) A system comprising:  
 2                   a computer system; and  
 3                   a design environment incorporated in the computer for providing tools to  
 4           facilitate determining optimal values of design parameters of a subsystem to satisfy  
 5           design constraints, the subsystem having a plurality of circuits.

1           22.    (TWICE AMENDED) [The system of claim 21 wherein the computer  
 2           system comprises] A system comprising:  
 3                   a memory for storing program instructions;  
 4                   a processor coupled to the memory [for executing] to execute the program  
 5           instructions, the program instructions when executed by the processor interacting  
 6           with [the] tools provided by [the] a design environment causing the processor to at  
 7           least

8                   (a)     create parameter functions for [the] a plurality of circuits in  
 9                   [the] a subsystem, the subsystem having design constraints, each one of the  
 10                  parameter functions corresponding to each one of the circuits, the parameter  
 11                  functions representing a relationship among the design parameters, [and]

12                   (b)     select initial design points for the parameter functions to  
 13                  satisfy the design constraints; and

14 [(b) optimize the design parameters based on the parameter  
 15 functions to satisfy] (c) select new design points for the parameter functions  
 16 to optimize design parameters within the design constraints.

1 23. (AMENDED) The system of claim 22 wherein the [parameter functions are  
 2 created by] program instructions causing the processor to create the parameter functions  
 3 causes the processor to:

4 (a1) [configuring] configure each circuit of the plurality of circuits; and

5 (a2) [generating] generate values of design parameters for each circuit  
 6 according to the configured circuit, the values providing the parameter functions.

1 24. The system of claim 22 wherein the design parameters include constraint  
 2 and optimizing sets, the constraint set including constraint parameters having values  
 3 selectable to meet the design constraints, the optimizing set including optimizing  
 4 parameters having values to be optimized.

1 25. (AMENDED) The system of claim 24 wherein the [design parameters are  
 2 optimized by] program instructions causing the processor to select the new design points  
 3 causes the processor to:

4 [(b1) selecting] (c1) select values of the constraint parameters to meet the  
 5 design constraints;

6                    [(b2) determining] (c2) determine values of the optimizing parameters  
 7                    corresponding to the selected values of the constraint parameters based on the  
 8                    parameter functions; and

9                    [(b3) iterating (b1)] (c3) iterate (c1) and [(b2)] (c2) until values of the  
 10                    optimizing parameters are within a predetermined optimal range.

1                    26.     The system of claim 24 wherein the constraint parameters include a delay  
 2                    parameter and the optimizing parameters include a power parameter.

1                    27.     The system of claim 26 wherein the design constraints include a delay  
 2                    constraint.

**CONCLUSION**

Applicant is respectfully requesting the above amendments to the title, abstract and claims prior to examination of the above-identified application.

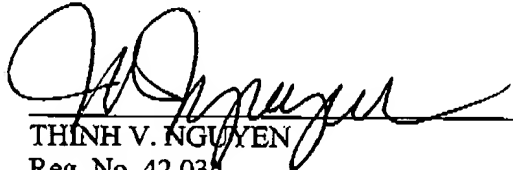
In view of the foregoing, favorable consideration and allowance of this application are respectfully solicited.

Applicant's undersigned attorney may be reached at the Costa Mesa office by telephone at (714) 557-3800. All correspondence should continue to be directed to the below-listed address.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: April 9, 2001

  
THINH V. NGUYEN  
Reg. No. 42,034

12400 Wilshire Boulevard, Seventh Floor  
Los Angeles, California 90025  
(714) 557-3800

**CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)**

I hereby certify that this correspondence is, on the date shown below, being:

**MAILING**

to be deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

**FACSIMILE**

to be transmitted by facsimile to the Patent and Trademark Office.

Name

Date

  
Rose Dunne

04/09/01  
Date